Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1-14 and 17 as follows:

Listing of Claims:

1.   (Amended)   A cache system comprising:

at least one DRAM array divided into a plurality of blocks;

first and second SRAM arrays each having a capacity at least as large as the capacity of a block of the <u>at least one</u> DRAM array;

an address decoder coupled to receive a memory address and being operable to decode the address and generate decoded address signals corresponding thereto;

an input/output circuit coupled to the <u>at least one</u> DRAM array, the <u>first and second</u> SRAM array<u>s</u>, and the address decoder, the input/output circuit being operable to respond to a first control signal by coupling write data from an external data terminal to a location in a block of the <u>at least one</u> DRAM array corresponding to the decoded address signals, or to respond to a second control signal by coupling write data from the external data terminal to a location in ~~the~~ <u>one of the</u> first ~~or~~ <u>and</u> second SRAM arrays, or to respond to a third control signal by coupling data from one of the <u>first and second</u> SRAM arrays to a location in a block of the <u>at least one</u> DRAM array corresponding to the decoded address signals; and

a control circuit coupled to the <u>at least one</u> DRAM array, the <u>first and second</u> SRAM array<u>s</u>, the address decoder, and the input/output circuit, the control circuit being operable to refresh the <u>at least one</u> DRAM array one block at a time, the control circuit further being operable to generate the first control signal when the block of the <u>at least one</u> DRAM array corresponding to the decoded address signals is not being refreshed, to generate the second control signal when the block of the <u>at least one</u> DRAM array corresponding to the decoded address signals is being refreshed, to generate the third control signal when the block of the <u>at least one</u> DRAM array that was being refreshed when the data was stored in <u>one of</u> the <u>first and second</u> SRAM array<u>s</u> is no longer being refreshed.

2.   (Amended)   The cache system of claim 1 wherein the control circuit comprises:

a refresh controller coupled to the at least one DRAM array, the refresh controller being operable to refresh the at least one DRAM array one block at a time; and

a control buffer structured to receive a memory command and to generate the first, second and third control signals corresponding thereto.

3.   (Amended)   The cache system of claim 1 wherein the plurality of blocks of the at least one DRAM array are physically part of a single DRAM array.

4.   (Amended)   The cache system of claim 1 wherein the an input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the at least one DRAM array while a second pair of input/output lines may be coupled to another block of the at least one DRAM array.

5.   (Amended)   A cache system comprising:

at least one DRAM array divided into a plurality of blocks;

first and second SRAM arrays each having a capacity at least as large as the capacity of a block of the at least one DRAM array, the first and second SRAM arrays being coupled to the at least one DRAM array for direct transfer of data from either of the first and second SRAM arrays to any block of the at least one DRAM array if the block of the at least one DRAM array is not being refreshed; and

an input/output circuit coupled to the at least one DRAM array and the first and second SRAM arrays, the input/output circuit being operable to store write data in a block of the at least one DRAM array to which the write data was directed, and to store write data directed to any block of the at least one DRAM array in either of the first and second SRAM arrays if the block to which the write data was directed is being refreshed.

6.   (Amended)   The cache system of claim 5 wherein the plurality of blocks of the at least one DRAM array is are physically part of a single DRAM array.

7.   (Amended)   The cache system of claim 5 wherein the an input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the at least one DRAM array while a second pair of input/output lines may be coupled to another block of the at least one DRAM array.

8.   (Amended)   A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a system controller coupled to the processor bus;

a system memory coupled to the processor through the system controller; and

a cache system coupled to the processor bus, the cache system comprising:

at least one DRAM array divided into a plurality of blocks;

first and second SRAM arrays each having a capacity at least as large as the capacity of a block of the at least one DRAM array;

a data transfer circuit coupled to the at least one DRAM array and the first and second SRAM arrays, the data transfer circuit being operable to respond to a first control signal by coupling write data to one of the first or and second SRAM arrays, or to respond to a second control signal by coupling data from one of the first and second SRAM arrays to a location in a block of the at least one DRAM array; and

a control circuit coupled to the at least one DRAM array and the first and second SRAM array, the control circuit being operable to refresh the at least one DRAM array one block at a time, the control circuit further being operable to generate the first control signal when the block of the at least one DRAM array to which write data is being directed is being refreshed, and to generate the second control signal when the block of the at least one DRAM array that was being refreshed when the data was stored in the at least one of the first and second SRAM arrays is no longer being refreshed.

9.   (Amended)   The computer system of claim 8 wherein the control circuit comprises:

a refresh controller coupled to the at least one DRAM array, the refresh controller being operable to refresh the at least one DRAM array one block at a time; and

a control buffer structured to receive a memory command and to generate the first, and second and third control signals corresponding thereto.

10.   (Amended)   The computer system of claim 8 wherein the plurality of blocks of the at least one DRAM array are physically part of a single DRAM array.

11.   (Amended)   The computer system of claim 8 wherein the an input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the at least one DRAM array while a second pair of input/output lines may be coupled to another block of the at least one DRAM array.

12.   (Amended)   A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a system controller coupled to the processor bus;

a system memory coupled to the processor through the system controller; and

a cache system coupled to the processor bus, the cache system comprising:

at least one DRAM array divided into a plurality of blocks;

first and second SRAM arrays each having a capacity at least as large as the capacity of a block of the at least one DRAM array;

an input/output circuit coupled to the at least one DRAM array and the first and second SRAM arrays, the input/output circuit being operable to write data

directed to any block of the <u>at least one</u> DRAM array in either of the <u>first and second</u> SRAM arrays if the block to which the write data was directed is being refreshed; and

a control circuit coupled to the <u>at least one</u> DRAM array and the <u>first and second</u> SRAM array<u>s</u>, the control circuit being operable to cause either of the <u>first and second</u> SRAM arrays to transfer data stored in the <u>one of the fist and second</u> SRAM array<u>s</u> to any block of the <u>at least one</u> DRAM array if the block of the <u>at least one</u> DRAM array is no longer being refreshed.

13.   (Amended)   The computer system of claim 12 wherein the <u>plurality of</u> block<u>s</u> of <u>the at least one</u> DRAM array <u>is</u> are physically part of a single DRAM array.

14.   (Amended)   The computer system of claim 12 wherein the an input/output circuit comprises a plurality of complimentary input/output line pairs, the input/output lines being sufficient in number that a first pair of input/output lines may be coupled to one block of the <u>at least one</u> DRAM array while a second pair of input/output lines may be coupled to another block of the <u>at least one</u> DRAM array.

15.   (Original)   A method of caching data, comprising:
providing a DRAM having a plurality of blocks each of which may be refreshed;
providing first and second SRAMs having a capacity of at least the capacity of the DRAM blocks;
addressing a first block of the DRAM in an attempt to write data into the first block of the DRAM;
if the first block of the DRAM is being refreshed during the attempt, writing the data into the first SRAM;
after the first block of the DRAM is no longer being refreshed, transferring data stored in the first SRAM to the first block of the DRAM;
addressing a second block of the DRAM in an attempt to write data into the second block of the DRAM;

if the second block of the DRAM is being refreshed during the attempt, and data is being transferred from the first SRAM to the first block of the DRAM, writing the data into the second SRAM; and

after the second block of the DRAM is no longer being refreshed, transferring data stored in the second SRAM to the second block of the DRAM.

16.   (Original)   The method of claim 15 further comprising writing data into the first SRAM if the second block of the DRAM is being refreshed during the attempt to write the data into the second block and data is not being transferred from the first SRAM to the first block of the DRAM.

17.   (Amended)   The method of claim 15 further comprising writing the data into the first <u>block</u> of the DRAM if the first block of the DRAM is not being refreshed during the attempt.

18.   (Original)   The method of claim 15 further comprising:

addressing a third block of the DRAM in an attempt to write data into the third block of the DRAM;

if the third block of the DRAM is being refreshed during the attempt, and data is being transferred from the second SRAM to the second block of the DRAM, writing the data into the first SRAM; and

after the third block of the DRAM is no longer being refreshed, transferring data stored in the first SRAM to the third block of the DRAM.

19.   (Original)   The method of claim 15 further comprising:

addressing a first block of the DRAM in an attempt to read data from the first block of the DRAM; and

outputting data from the first block of the DRAM.

20.   (Original)   The method of claim 19 wherein the act of outputting data from the first block of the DRAM is accomplished regardless of whether or not the first block of memory is being refreshed.

21.   (Original)   The method of claim 15 further comprising:

addressing the first block of the DRAM in an attempt to read data from the first block of the DRAM; and

outputting data from the first block of the DRAM; and

caching the data output from the first block of the DRAM in the first SRAM.

22.   (Original)   The method of claim 21 further comprising

addressing the first block of the DRAM in an attempt to read data from the first block of the DRAM; and

outputting data from the first block of the first SRAM.

23.   (Original)   A method of caching data, comprising:

providing a DRAM having a plurality of blocks each of which may be refreshed;

providing first and second SRAMs having a capacity of at least the capacity of the DRAM blocks;

sequentially attempting to write data to blocks of the DRAM;

if a block to which data is attempting to be written is being refreshed, writing the data to one of the SRAMs;

when the refresh of a block has been completed, transferring data from the SRAM to which the data had been written to a block of the DRAM to which data was attempted to be written; and

if a block to which data is attempting to be written is being refreshed and data is being transferred from the one SRAM to a block of the DRAM, writing the data to the other SRAM.

24. (Original) The method of claim 23 further comprising, if the block to which data is attempting to be written is not being refreshed, writing the data to the block of the DRAM.

25. (Original) The method of claim 23 further comprising:

attempting to read data from a block of the DRAM; and

outputting data from the block of the DRAM to which an attempt to read data is directed.

26. (Original) The method of claim 25 wherein the act of outputting data from the block of the DRAM is accomplished regardless of whether or not the block of memory is being refreshed.

27. (Original) The method of claim 25 further comprising:

attempting to read data from a block of the DRAM;

outputting data from the block of the DRAM to which an attempt to read data is directed and

caching the data output from the block of the DRAM in one of the SRAMs.